CLAIMS

WHAT IS CLAIMED IS:

1. A method of manufacturing an integrated circuit, comprising:

providing a gate structure between a source location and a drain location in a semiconductor substrate;

providing an angled source extension implant in a direction from the source location to the drain location;

providing an angled drain extension implant in a direction from the drain location to the source location; and

providing a deep source/drain implant at the source location and the drain location.

2. The method of claim 1, further comprising providing a pair of spacers abutting lateral sides of the gate structure before the deep source drain implant.

3. The method of claim 2, wherein the providing the source extension step is a low energy, high dose ion implantation step.

4. The method of claim 3, wherein the drain extension implant step is a medium energy, high dose ion implantation step.

5. The method of claim 4, wherein a source extension formed by the source extension step is shallower than a drain extension formed by the drain extension implant step.

6. The method of claim 5, wherein the source extension has approximately 5 times the concentration of dopants of the drain extension.

7. The method of claim 5, wherein the source extension has a concentration of $5x10^{19}$-$1x10^{20}$ of dopants per centimeter cubed and the drain extension has a concentration of $1x10^{19}$-$5x10^{19}$ dopants per centimeter cubed.

8. The method of claim 5, wherein the drain extension has a concentration between $1x10^{19}$ - $5x10^{19}$ dopants per centimeter cubed.

9. The method of claim 5, wherein the drain extension is more than 80 nm deep.

10. The method of claim 7, wherein the gate structure is associated with a N-channel or P-channel with MOSFET.

11. A method of manufacturing an ultra-large scale integrated circuit including a plurality of field effect transistors, the method comprising steps of:

providing at least part of a gate structure on a top surface of a semiconductor substrate;

forming a source extension with dopants of a first conductivity type;

forming a drain extension with dopants of the first conductivity type; and

forming deep source and drain regions with dopants of the first conductivity type, wherein the gate structure is between the source and drain regions, wherein the drain extension is deeper than the source extension.

12. The method of claim 11, wherein the forming source and drain regions further comprises:

providing a pair of spacers abutting lateral sides of the gate structure; and

providing a deep source/drain implant at the source location and the drain location.

13. The method of claim 11, wherein the drain extension is formed in a low dosage implant process.

14. The method of claim 11, wherein the source extension is formed at an energy level of between 1-5 KeV.

15. The method of claim 11, wherein the drain extension is formed at an energy level of between 5-15 KeV.

16. The method of claim 11, wherein the first conductivity type is N-type.

17. The method of claim 11, wherein the first conductivity type is P-type.

18. An integrated circuit including a plurality of field effect transistors, each of the transistors comprising:

a gate structure disposed over a channel;

a deep source region heavily doped with dopants of a first conductivity type;

a deep drain region heavily doped with dopants of the first conductivity type;

a source extension integral the deep source region; and

a drain extension integral the deep drain region, wherein the drain extension is deeper than the source extension.

19. The integrated circuit of claim 18, wherein the source extension is more heavily doped than the drain extension.

20. The integrated circuit of claim of claim 19, wherein the drain extension is more than 80 nm thick and the source extension is less than 40 nm thick.